Docket No.: GR 98 P 5874

CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of application number 09/873,227, filed June 4, 2001.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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A ~~Description~~

Power semiconductor switch

ins A1 ~~The present invention relates to an IGBT (Insulated Gate~~ Bipolar Transistor) ~~which is~~ suitable for forming bidirectional switches.

ins A2

Commercially available IGBTs can be used to construct bidirectional switches which are used e.g. in converters, by each IGBT being connected in series with a diode. In this case, the forward direction of the diode corresponds to the switchable current direction of the IGBT. This circuit therefore effects blocking in the reverse direction. However, high on-state losses have to be accepted with this. US 5,608,237 describes a bidirectional semiconductor switch comprising IGBTs in which IGBT structures are formed on two mutually opposite main sides of a semiconductor body. The dimensioning of such proposals for bidirectionally blocking switches is in each case chosen in such a way as to produce an NPT component (Non Punch Through). A triangular field profile builds up in the component under blocking loading. Other symmetrically blocking components such as e.g. thyristors or GTOs likewise have a non-punch-through dimensioning. That

requires the component to have a large thickness and thus increases the switching and on-state losses in relation to the thinner punch-through dimensioning.

no. A3 ~~It is an object of the present invention to specify a simply designed switch which can block high voltages in both directions. This object is achieved by means of the component having the features of claim 1. Refinements emerge from the dependent claim.~~ A

In the case of the component according to the invention, a conventional structure of a power semiconductor switch, e.g. of an IGBT, is provided with an additional buffer layer on the source side and dimensioned in such a way that, in an operating state in which the component effects blocking, at least in a range of high electrical voltages which are applied to source and drain, a space charge zone produced in the semiconductor body extends as far as the respective buffer layer in accordance with a punch-through dimensioning. By virtue of the buffer layers present on both sides, the advantage of punch-through dimensioning (small thickness of the component) is combined with the advantage of non-punch-through dimensioning (possibility of symmetrical blocking capability).

ins A4

~~The component according to the invention is described in more detail below using the example illustrated in cross section in the figure.~~ A

ins A5

A detail from an IGBT structure is illustrated in cross section on the right-hand side of the figure. A first base region 1 is essentially formed by the semiconductor body provided with a basic doping. This basic doping is preferably a doping for weak n-type conductivity. In accordance with an IGBT structure known per se, a second base region 4 of opposite sign and emitter regions 3, 5 are present. The sequence of these regions has conductivities having alternating signs in the vertical direction. In the second base region 4, which is formed in a manner extending as far as the top side of the semiconductor body, a channel is formed on said top side, which channel can be controlled by means of a gate electrode G applied above it and preferably isolated from it by a dielectric. The second base region 4 is preferably formed as a p-conducting doped well in the n^--conducting doped semiconductor body. Situated within this well is the region 5 doped oppositely thereto (in this example n-conducting), said region being connected to the source contact S, which also makes contact with the second base region 4. Situated on the rear side of the component is a further doped region 3, which, as emitter region, is doped oppositely to the first base region 1 and is provided with a drain contact D. In accordance

with a punch-through dimensioning known per se, the thickness of the semiconductor body is chosen to be smaller than in IGBTs with non-punch-through dimensioning, and a buffer layer 2 whose conductivity has the same sign as that of the first base region 1 is arranged between the first base region 1 and the region provided with the drain contact (p-type emitter). This buffer layer 2 is preferably doped with a dose of $1 \cdot 10^{12}$ cm^{-2} to $4 \cdot 10^{12}$ cm^{-2} (integral over the doping profile). In the blocking operating state of the component, in contrast to the conventional layer structure with buffer layer, the electric field for the most part falls in the first base region 1. A typical profile of the electric field in the vertical direction of the component is illustrated on the left-hand side of the figure for the case where the drain terminal is positive relative to the source terminal (solid curve in the y-E diagram).

What is essential to the invention is a further buffer layer 6, which is present between the first base region 1 and the second base region 4 and is doped such that its electrical conductivity has the same sign as that of the first base region 1 (basic doping of the semiconductor body). This further buffer layer 6, which is n-conducting in this example, is doped so highly (most preferably with a dose of $1 \cdot 10^{12}$ cm^{-2} to $4 \cdot 10^{12}$ cm^{-2}) that, in the event of polarity reversal of the voltage between drain and source, a profile of the

electric field in the vertical direction of the component is produced which, in principle, corresponds to the broken curve depicted in the diagram on the left-hand side of the figure. To an extent, the punch-through case for the opposite direction is present here, with the result that this component also blocks high voltages in both directions. The blocking operating state is changed over, in a manner known per se, into the operating state open from source to drain, by means of the control of the channel via the gate electrode. Therefore, according to the invention, a component is present which constitutes a switch in a current direction and blocks the current in the opposite direction up to high voltages.

The basic doping of the semiconductor body is preferably chosen to be somewhat lower than is otherwise customary (e.g., for 1200 V IGBTs, 90 Ωcm instead of 60 Ωcm). The thickness and the magnitude of the doping in the first base region 1 and the two buffer layers 2, 6 must be accurately dimensioned; in the case of an excessively high doping and/or thickness of the layers, a premature breakdown takes place on account of the avalanche multiplication of the charge carriers (avalanche effect) and, in the case of an excessively low doping of the buffer layers, a breakdown takes place on account of punch-through of the blocked PNP transistor. In the case of correct dimensioning, which can easily be found using the customary procedures for the respective exemplary embodiment, it is

possible to reduce the thickness of the component. In addition, the further buffer layer 6 under the p-conducting doped well in the semiconductor body brings about an elevation of the charge carrier density in this region, with the result that the switching losses are reduced and an improvement by approximately 30 - 40% with the on-state losses remaining the same is possible. As a result, it is possible to realize a symmetrically blocking 1200 V IGBT, and likewise symmetrically blocking thyristors or GTOs.